[0066] The first adjustment stage ER**1** furthermore comprises a first stabilization module MS**1** known per se to the person skilled in the art and configured to stabilize the first adjustment stage ER**1**.

[0067] Thus, the gate source voltage of the switching transistor TC is decreased in such a way as to reduce the positive inrush current CE+ flowing from the input terminal BE to the output terminal BS.

[0068] By analogy, reference is now made to FIG. **4** to schematically illustrate an exemplary embodiment of the second adjustment stage ER**2**.

[0069] The second adjustment stage ER**2** comprises

[0070] a second detection capacitor CD**2** coupled to the output voltage VOUT and configured to transform a negative variation of the output voltage VOUT into a variation of a second internal current Iint**2**,

[0071] a second current mirror module MMC**2** comprising here, for example, a second current mirror MCP of the pMOS type and a second current mirror MCN of the nMOS type which are known per se and respectively having current transfer ratios equal to 0 and P,

[0072] a second reference current module MCR**2** configured to generate the second reference current Iref**2**, and

[0073] a second voltage adjustment module MRT**2** comprising

[0074] a second transistor TC**2** of the pMOS type whose gate is coupled to the output of the second reference current module MCR**2** and to the output of the second current mirror module MMC**2**, and whose source is coupled to the larger of the input VIN and output VOUT voltages and whose drain is coupled to the gate G of the switching transistor TC.

[0075] By way of indication, the charge switch circuit **3** can receive a reference current, for example, a current proportional to the absolute temperature ("proportional to absolute temperature current"), which is copied to create the currents of the reference current source SCR, of the first source current module MCR**1** and of the second reference current module MCR**2**.

[0076] The second current mirror MCP of the pMOS type comprises a current mirror pMOS transistor TPMC arranged diode-fashion whose drain is coupled to the ground GND via an auxiliary transistor TAN of the nMOS type.

[0077] At its gate, the transistor TAN receives a signal SA**2** complementary to the second activation signal SA**2**. When the second activation signal SA**2** is in the low state, the complementary signal SA**2** is in the high state. The transistor TAN is consequently in its "on" state. The transistor TPMC is thus biased via the ground GND.

[0078] When the second activation signal SA**2** is in the high state, the complementary signal SA**2** is in the low state. The transistor TAN is in its "off" state. The negative variation of the voltage VOUT is transformed into the variation of the second internal current Iint**2** via the second detection capacitor CD**2**.

[0079] The second current mirror MCN of the nMOS type comprises a second current mirror nMOS transistor TNMC**2** arranged diode-fashion whose drain is coupled to the battery voltage VBAT via a second auxiliary transistor TAP**2** of the pMOS type.

[0080] Just as described hereinabove for the first current mirror nMOS transistor TNMC**1** and the first auxiliary transistor TAP**1**, the transistor TAP**2** is configured to be in the "on" state when the second activation signal SA**2** is in the low state in such a way as to allow the transistor TNMC**2** to be biased by the battery voltage VBAT.

[0081] The second current mirror module MMC**2** is consequently in operation by virtue of the biasing of the transistor TPMC via the transistor TAN and the biasing of the transistor TNMC**2** via the transistor TAP**2** when the second activation signal SA**2** is in the low state.

[0082] These dynamic structures advantageously allow activation of the second adjustment stage ER**2** only when the second activation signal SA**2** is in the high state.

[0083] It should be noted that the first or the second activation signal SA**1** or SA**2** is set just at the moment at which one needs to activate the first or the second adjustment stage ER**1** or ER**2** since the first and second adjustment stages ER**1** and ER**2** comprise the dynamic structures, as described hereinabove.

[0084] The second current mirror module MMC**2** is configured to generate a second intermediate current O*P*Iint**2** on the basis of the second internal current Iint**2**. It should be noted that the second current mirror MCP of the pMOS type is particularly configured to generate a current O*Iint**2** whose direction is suited to the generation of the second intermediate current O*P*Iint**2** via the second current mirror MCN of the nMOS type.

[0085] If the second intermediate current O*P*Iint**2** becomes greater than the second reference current Iref**2**, the voltage of the gate of the second transistor TC**2** decreases and the voltage of the gate VG of the switching transistor TC is therefore pulled upwards.

[0086] Moreover, the second adjustment stage ER**2** comprises a second stabilization module MS**2** known per se to the person skilled in the art and configured to stabilize the second adjustment stage ER**2**.

[0087] Thus, the gate source voltage of the switching transistor TC is decreased in such a way as to reduce the negative inrush current CE− flowing from the output terminal BS to the input terminal BE.

[0088] The invention is not limited to the embodiments which have just been described but embraces all variants thereof.

[0089] By way of non-limiting example, the first and second reference current modules (MCR**1**, MCR**2**) may be substantially identical.

[0090] Furthermore, the first and second reference currents (Iref**1**, Iref**2**) may be substantially identical, and the first and second voltage adjustment modules (MRT**1**, MRT**2**) may be substantially identical.

What is claimed is:

1. A circuit having a first voltage at a first terminal and a second voltage at a second terminal, the circuit comprising:

a first adjustment stage circuit configured to limit a positive inrush current flowing between the first terminal and the second terminal;

a second adjustment stage circuit configured to limit a negative inrush current flowing between the first terminal and the second terminal; and

a control circuit configured to activate one of the first adjustment stage circuit or the second adjustment stage circuit based on a voltage difference between the first voltage and the second voltage.

2. The circuit of claim **1**, wherein the first adjustment stage circuit is activated in response to the first voltage being greater than the second voltage.